PATENT APPLICATION
Docket No. 5484-093
Client No. PX1392-US/SSD

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Byeong-Hoon Lee and Seung-Keun Lee		
Serial No.	09/997,080	Examiner:	Phan, Trong Q
Filed:	November 28, 2001	Art Unit:	2818
For:	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE		
Confirmation No.:	6095		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF UNDER 37 CFR §1.192

Appeal is taken from the Examiner's Office Action mailed July 31, 2003, finally rejecting claims 1-20 and 26-27 in the instant application.

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on October 29, 2003, and received by the OIPE on November 3, 2003.

The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees therefor are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This Brief is transmitted in triplicate.

This Brief contains these items under the following headings, and in the order set forth below.

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I. REAL PARTY IN INTEREST

37 CFR §1.192(c) (1)

The real party in interest is:

Samsung Electronics Co., Ltd.
416 Maetan-dong, Paldal-ku, Suwon-City
Kyungki-do KOREA

II. RELATED APPEALS AND INTERFERENCES

37 CFR §1.192(c) (2)

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the appellant's legal representative.

III. STATUS OF CLAIMS

37 CFR §1.192(c) (3)

1. Claims presented: 1-27.
2. Claims withdrawn from consideration but not cancelled: NONE
3. Claims not entered: 21-25
4. Claims canceled: NONE
5. Claims pending: 1-20, 26, 27

   of which:

   a. claims allowed: NONE

   b. claims rejected: 1-20, 26, 27

All the rejected claims, namely claims 1-20, 26, and 27 are being appealed. The appealed claims are eligible for appeal, having been finally rejected.

IV. STATUS OF AMENDMENTS
37 CFR §1.192(c) (4)

Subsequent to the last Office Action mailed on July 31, 2003, which contained a Final rejection of the appealed claims, no amendment has been filed.

V. SUMMARY OF THE INVENTION
37 CFR §1.192(c) (5)

Embodiments of the invention provide a non-volatile semiconductor memory device that includes a substrate (FIG. 4, element 1) and a plurality of sectors on the substrate. Each sector (FIGS. 3 and 4, element 100) includes memory cell transistors (FIGS. 3 and 4; elements M1 – Mn; M11 – Mn1; M1m – Mnm) in a cell array block (FIGS. 3 and 4; element 101) and decoder transistors (FIGS. 3 and 4; elements T1-T3) in a column decoder block (FIGS. 3 and 4; element 103). The transistors in the cell array block and the column decoder block share a common bulk region (FIG. 4; element 10) formed on the substrate (FIG. 4; element 1) and connected to a bulk driver (FIG. 3; element 400). There is a bulk driver (FIG. 3; element 400) provided for each of the sectors.

FIGS. 3 and 4 are described in the written specification at page 6, line 31 to page 7, line 28.

VI. ISSUES ON APPEAL
37 CFR §1.192(c) (6)

A. Whether claims 1-4 and 26 are anticipated under 35 U.S.C. §102(b) by USPN 5,994,732 to Ajika et al. (hereafter, 'Ajika'). See Examiner's Final Action, ¶ 2.

B. Whether claims 5-9 are anticipated under 35 U.S.C. §102(b) by Ajika.

C. Whether claims 10-14 are anticipated under 35 U.S.C. § 102(b) by Ajika.

D. Whether claims 15-17 and 27 are anticipated under 35 U.S.C. § 102(b) by Ajika.

E. Whether claims 18-20 are anticipated under 35 U.S.C. § 102(b) by Ajika.

VII. GROUPING OF CLAIMS
37 CFR §1.192(c) (7)

A. First Ground of Rejection

Claims 1-4 and 26 are rejected under 35 U.S.C. §102(b) as anticipated by Ajika. The claims of this group do not stand or fall together.

B. Second Ground of Rejection

Claims 5-9 are rejected under 35 U.S.C. §102(b) as anticipated by Ajika. The claims of this group do not stand or fall together.

C. Third Ground of Rejection

Claims 10-14 are rejected under 35 U.S.C. §102(b) as anticipated by Ajika. The claims of this group do not stand or fall together.

D. Fourth Ground of Rejection

Claims 15-17 and 27 are rejected under 35 U.S.C. §102(b) as anticipated by Ajika. The claims of this group do not stand or fall together.

E. Fifth Ground of Rejection

Claims 18-20 are rejected under 35 U.S.C. §102(b) as anticipated by Ajika.

VIII. ARGUMENT
37 CFR §1.192(c) (8)

With respect to claim group A (claims 1-4 and 26), claim 1 recites a nonvolatile semiconductor memory device including, *inter alia*, a plurality of sectors, each sector comprising memory cell transistors arranged in a cell array block. Another feature of claim 1 is that the semiconductor memory device is configured to electrically erase all of the memory cell transistors in a sector together.

It has been alleged that these features are disclosed by Ajika FIG. 8. In particular, it is alleged that p-well regions 3a (column 2, lines 49-50) correspond to the recited "plurality of sectors" and that one of the erase blocks 26 corresponds to the recited "cell array block."

However, it is clear from FIG. 8 that the p-well regions 3a include a number of erase blocks 26. Ajika teaches that only the memory cell transistors belonging to a single erase block 26 in the p-well region 3a is configured to be collectively erased (column 2, lines 49-52). Thus, Ajika FIG. 8 does not teach the recited claim 1 feature that the memory device is configured to electrically erase all of the memory cell transistors in a sector together.

Ajika admits that FIG. 8 is prior art and teaches that there is a serious disadvantage to using the structure of FIG. 8 (column 2, line 62 to column 3, line 28). Ajika FIG. 1, which illustrates Ajika's invention, is actually the more appropriate structure to consider with respect to claim 1.

In FIG. 1, Ajika shows that one erase block 26 is arranged in each p-well region 3 (column 6, lines 1-2).

However, claim 1 also recites the feature that each sector also comprises decoder transistors (plural) in a column decoder block (singular), in addition to memory transistors

arranged in a cell array block.

Contrary to this recited feature, Ajika teaches that two select gate transistors 12 are provided in the p-well region 3, one on each end of the p-well region (FIGS. 2 and 3; column 6, lines 52-58). Thus, if Ajika's select gate transistors 12 correspond to the recited decoder transistors, they are not arranged in a column decoder block as recited in claim 1.

Consequently, Ajika fails to anticipate claim 1 because it does not teach each and every element recited in claim 1 (MPEP 2131). Claims 2-4 and 26 inherently contain the features of claim 1. Consequently, Ajika fails to anticipate claims 2-4 and 26 for the same reason that it fails to anticipate claim 1.

Furthermore, it is believed that claim 4 and claim 26 contain subject matter that is allowable over Ajika.

Claim 4 recites that the write driver and the sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 4 for this additional reason (MPEP 2131).

Claim 26 recites that the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines. To the contrary, Ajika teaches that "erase block 26 is preferably defined to include all of a plurality of memory transistors sharing ***one*** word line in one erase block 26" (FIG. 2; column 7, lines 61-67; emphasis added). To anticipate a claim, the identical invention must be shown in as complete detail as is contained in the claim (see, e.g., MPEP 2131). Ajika does not show the recited feature of claim 26, consequently Ajika does not anticipate claim 26 for this additional reason (MPEP 2131).

With respect to claim group B (claims 5-9), claim 5 recites, similar to claim 1, a sector structure comprising, *inter alia*, a plurality of decoder transistors arranged in a column decoder block.

Contrary to this recited feature, Ajika teaches that two select gate transistors 12 are provided in the p-well region 3, one on each end of the p-well region (FIGS. 2 and 3; column 6, lines 52-58). Thus, if Ajika's select gate transistors 12 correspond to the recited decoder transistors, they are not arranged in a column decoder block as recited in claim 5.

Consequently, Ajika fails to anticipate claim 5 because it does not teach each and every element recited in claim 5 (MPEP 2131). Claims 6-9 inherently contain the features of claim 5. Consequently, Ajika fails to anticipate claims 6-9 for the same reason that it fails to

anticipate claim 5.

Furthermore, it is believed that claims 7 and 8 contain subject matter that is allowable over Ajika.

Claim 7 recites, *inter alia*, that the sector structure further comprises a plurality of word lines arranged in the cell array block. Contrary to this recited feature, Ajika teaches that an erase block 26 is defined to include all of a plurality of memory transistors sharing **one** word line in one erase block 26 (FIG. 2; column 7, lines 61-67; emphasis added). Consequently, Ajika fails to anticipate claim 7 for this additional reason (MPEP 2131).

Claim 8 recites, inter alia, that the write driver and the sense amplifier are configured to be placed in a state of high impedance during an erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 8 for this additional reason (MPEP 2131).

With respect to claim group C (claims 10-14), claim 10 recites, *inter alia*, a nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising a cell array block and a column decoder block. The cell array block further comprises a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate connected to a corresponding word line out of the plurality of word lines, each drain connected to a corresponding bit line out of the plurality of bit lines.

Contrary to claim 10, Ajika's erase block 26 does not comprise a plurality of bit lines, rather there is only one main bit line 24 that is connected to the select gate transistors that are located on either side of the erase block (FIGS. 2 and 3; column 7, lines 15-20). Ajika discloses that sub bit lines 19a, 19b are connected to the drains 4 of ***each*** memory transistor 11 (FIG. 2 and 3; column 6, lines 63-65; emphasis added). However, if the sub bit lines 19a, 19b are considered to be the recited plurality of bit lines then the drains of each of the memory cell transistors are not connected to a corresponding bit line out of the plurality of bit lines as recited in claim 10.

Also contrary to claim 10, Ajika's erase block 26 does not comprise a plurality of word lines (FIG. 2; column 7, lines 61-67).

Claim 10 also recites that the column decoder block further comprises a plurality of column decoder transistors, each column decoder transistor connected between a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines.

It is alleged that the select gate transistors 12 within the memory erase blocks 26 are

the recited "column decoder block." In this case, the select gate transistors are provided at both ends of the p-well region 3, on either side of the erase block 26 (FIGS. 2 and 3; column 6, lines 52-67).

Pending claims must be interpreted consistently with the specification (see, e.g., MPEP 2111). The applicants submit that the interpretation of a "column decoder block" as being the select gate transistors 12 on both sides of the erase block 26 is inconsistent with the specification, where a "column decoder block" is shown in FIG. 3 as a singular, contiguous area 103, and not as plural areas separated by the erase block 26 as shown in Ajika FIG. 2 and 3. In other words, the applicants have claimed a single "column decoder block" having a plurality of column decoder transistors, and not multiple "column decoder blocks" that each have a single select gate transistor.

Furthermore, even if the two select gate transistors 12 shown at either side of the erase block in Ajika FIG. 2 and 3 could be considered a "column decoder block," each of Ajika's select gate transistors 12 is not connected to a corresponding bit line out of the plurality of bit lines as required by claim 10. Rather, both of Ajika's sub bit lines 19a, 19b are connected to one n-type impurity region 15b of the select gate transistor via a contact hole 17 (column 6, lines 65-67), while the other n-type impurity region 15a of the select gate transistor is connected to the main bit line 24 through a contact hole 16 (column 7, lines 17-20). In other words, only one main bit line 24 is connected to the select gate transistors 12 in Ajika's "column decoder block", not a plurality of bit lines. It was explained above why Ajika's sub bit lines 19a, 19b cannot be considered the recited plurality of bit lines.

Because Ajika fails to teach the elements of claim 10 discussed above, Ajika does not anticipate claim 10 (MPEP 2131). Claims 11-14 inherently contain the features of claim 10, consequently, claims 11-14 are also not anticipated by Ajika (MPEP 2131).

Furthermore, it is believed that claim 14 contains subject matter that is allowable over Ajika.

Claim 14 recites that the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 14 for this additional reason (MPEP 2131).

With respect to claim group D (claims 15-17 and 27), independent claim 15 has been alleged to be anticipated by Ajika FIG. 8. While the comments previously presented for claim 15 with respect to Ajika FIG. 8 still apply, the same comments can not be made with

respect to Ajika FIG. 1.

However, claim 17 recites that the transistors of the column decoder (claim 15) comprise a column decoder block. As was explained above, Ajika's select gate transistors 12 are found on opposite sides of the erase block 26, thus they cannot be considered the recited column decoder block. Consequently, Ajika fails to anticipate claim 17 (MPEP 2131). Assuming that this argument proves persuasive to the Board, the applicants propose amending claim 15 to incorporate this subject matter.

Furthermore, claim 27 recites that the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one. Ajika does not teach these features. For example, Ajika does not show a column decoder block arranged in at least a (1 x 2) array, neither does it show a cell array block arranged in at least a (2 x 2) array. Consequently, Ajika fails to anticipate claim 27 (MPEP 2131).

With respect to claim group E, claim 18 recites, similar to claim 27, a cell array block arranged in a (M x N) array, where M and N are at least equal to 2, and a column decoder block arranged in a (P x N) array, where P is at least equal to 1. Ajika does not teach this feature, consequently, Ajika fails to anticipate claim 18 (MPEP 2131).

Claims 19 and 20 inherently contain the features recited in claim 18. Consequently, Ajika fails to anticipate claims 19 and 20 for the same reason as claim 18.

IX. APPENDIX
37 CFR §1.192(c) (9)

1. (Previously presented) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sectors on the substrate;

each sector comprising memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block;

wherein the transistors in the cell array block and column decoder block in each sector share a common bulk region, wherein the common bulk region is formed on the substrate and is connected to a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of the sector; and

wherein said semiconductor memory device is configured to electrically erase all the

memory cell transistors in a sector together.

2. (Original) A nonvolatile semiconductor memory device according to claim 1, wherein the semiconductor memory device is a NOR-type memory device.

3. (Original) A nonvolatile semiconductor memory device according to claim 1, further comprising a write driver and a sense amplifier.

4. (Original) A nonvolatile semiconductor memory device according to claim 3, wherein the write driver and sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation.

5. (Original) A sector structure of a nonvolatile semiconductor memory, said sector structure comprising:

a plurality of memory cell transistors arranged in a cell array block; and

a plurality of decoder transistors arranged in a column decoder block, wherein said memory cell transistors and decoder transistors are arranged on a common bulk region.

6. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein an erase operation is configured to erase all of the transistors in the sector simultaneously.

7. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, said sector structure further comprising:

a plurality of word lines arranged in the cell array block, each word line being connected to a plurality of cell gates;

a plurality of bit lines arranged in the cell array block, each bit line being connected to a plurality of memory cell drains;

a plurality of common data lines connected to the bit lines;

a plurality of write drivers, each connected to a respective one of the common data lines; and

a plurality of sense amplifiers, each connected to a respective one of the common data

lines.

8. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 7, wherein each write driver and sense amplifier is configured to be placed in a state of high impedance during an erase operation.

9. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein said sector structure is configured to provide 64 Kbytes of memory.

10. (Previously Presented) A nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising:

a cell array block comprising a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of the plurality of word lines, each drain being connected to a corresponding bit line out of the plurality of bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors and configured to apply a source voltage;

a column decoder block comprising a plurality of column decoder transistors, each column decoder transistor connected a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines; and

a common bulk region arranged in each sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors in each sector share the common bulk region; and

a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

11. (Original) A nonvolatile semiconductor memory device according to claim 10, wherein the memory device is a NOR-type flash EEPROM.

12. (Original) A nonvolatile semiconductor memory device according to claim 10, wherein the bulk region is a pocket P-well.

13. (Original) A nonvolatile semiconductor memory device according to claim 10, further comprising a plurality of write drivers and sense amplifiers, wherein each data line is connected to a corresponding one of the write drivers and a corresponding one of the sense amplifiers.

14. (Original) A nonvolatile semiconductor memory device according to claim 13, wherein the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation.

15. (Previously presented) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sector units, each sector unit comprising a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, and wherein each sector unit is configured to be electrically erasable in response to an erase signal; and a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage.

16. (Original) A nonvolatile semiconductor memory device according to claim 15, wherein each sector unit further comprises a bulk driver configured to supply a bulk voltage to the common bulk region.

17. (Original) A nonvolatile semiconductor memory device according to claim 15, wherein said plurality of memory cell transistors are arranged in a cell array block, wherein said plurality of column decoder transistors are arranged in a column decoder block, and wherein said cell array block and said column decoder block are both arranged on the common bulk region.

18. (Previously presented) A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:

forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the cell array block is arranged in an (M x N) array with M and N both at least equal to two; and

forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder is arranged in a (P x N) array with P at least equal to one.

19. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, further comprising configuring the bulk regions for the memory cell transistors and decoder transistors to receive a common bulk signal during an erase operation.

20. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, wherein said memory cell transistors and said decoder transistors are configured to be simultaneously erased with each other during an erase operation.

21-25. (Not entered)

26. (Previously presented) The device of claim 1, wherein the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines.

27. (Previously presented) The device of claim 17, wherein the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one.

CONCLUSION

The Appellant requests favorable consideration by the Board. If any questions remain, please call the undersigned.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Date: January 2, 2004

Adrienne Chocholak

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FIGS. 3 and 4 are described in the written specification at page 6, line 31 to page 7, line 28.

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B. Whether claims 5-9 are anticipated under 35 U.S.C. §102(b) by Ajika.

C. Whether claims 10-14 are anticipated under 35 U.S.C. § 102(b) by Ajika.

D. Whether claims 15-17 and 27 are anticipated under 35 U.S.C. § 102(b) by Ajika.

E. Whether claims 18-20 are anticipated under 35 U.S.C. § 102(b) by Ajika.

VII. GROUPING OF CLAIMS
37 CFR §1.192(c) (7)

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D. Fourth Ground of Rejection

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E. Fifth Ground of Rejection

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VIII. ARGUMENT
37 CFR §1.192(c) (8)

With respect to claim group A (claims 1-4 and 26), claim 1 recites a nonvolatile semiconductor memory device including, *inter alia*, a plurality of sectors, each sector comprising memory cell transistors arranged in a cell array block. Another feature of claim 1 is that the semiconductor memory device is configured to electrically erase all of the memory cell transistors in a sector together.

It has been alleged that these features are disclosed by Ajika FIG. 8. In particular, it is alleged that p-well regions 3a (column 2, lines 49-50) correspond to the recited "plurality of sectors" and that one of the erase blocks 26 corresponds to the recited "cell array block."

However, it is clear from FIG. 8 that the p-well regions 3a include a number of erase blocks 26. Ajika teaches that only the memory cell transistors belonging to a single erase block 26 in the p-well region 3a is configured to be collectively erased (column 2, lines 49-52). Thus, Ajika FIG. 8 does not teach the recited claim 1 feature that the memory device is configured to electrically erase all of the memory cell transistors in a sector together.

Ajika admits that FIG. 8 is prior art and teaches that there is a serious disadvantage to using the structure of FIG. 8 (column 2, line 62 to column 3, line 28). Ajika FIG. 1, which illustrates Ajika's invention, is actually the more appropriate structure to consider with respect to claim 1.

In FIG. 1, Ajika shows that one erase block 26 is arranged in each p-well region 3 (column 6, lines 1-2).

However, claim 1 also recites the feature that each sector also comprises decoder transistors (plural) in a column decoder block (singular), in addition to memory transistors

arranged in a cell array block.

Contrary to this recited feature, Ajika teaches that two select gate transistors 12 are provided in the p-well region 3, one on each end of the p-well region (FIGS. 2 and 3; column 6, lines 52-58). Thus, if Ajika's select gate transistors 12 correspond to the recited decoder transistors, they are not arranged in a column decoder block as recited in claim 1.

Consequently, Ajika fails to anticipate claim 1 because it does not teach each and every element recited in claim 1 (MPEP 2131). Claims 2-4 and 26 inherently contain the features of claim 1. Consequently, Ajika fails to anticipate claims 2-4 and 26 for the same reason that it fails to anticipate claim 1.

Furthermore, it is believed that claim 4 and claim 26 contain subject matter that is allowable over Ajika.

Claim 4 recites that the write driver and the sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 4 for this additional reason (MPEP 2131).

Claim 26 recites that the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines. To the contrary, Ajika teaches that "erase block 26 is preferably defined to include all of a plurality of memory transistors sharing ***one*** word line in one erase block 26" (FIG. 2; column 7, lines 61-67; emphasis added). To anticipate a claim, the identical invention must be shown in as complete detail as is contained in the claim (see, e.g., MPEP 2131). Ajika does not show the recited feature of claim 26, consequently Ajika does not anticipate claim 26 for this additional reason (MPEP 2131).

With respect to claim group B (claims 5-9), claim 5 recites, similar to claim 1, a sector structure comprising, *inter alia*, a plurality of decoder transistors arranged in a column decoder block.

Contrary to this recited feature, Ajika teaches that two select gate transistors 12 are provided in the p-well region 3, one on each end of the p-well region (FIGS. 2 and 3; column 6, lines 52-58). Thus, if Ajika's select gate transistors 12 correspond to the recited decoder transistors, they are not arranged in a column decoder block as recited in claim 5.

Consequently, Ajika fails to anticipate claim 5 because it does not teach each and every element recited in claim 5 (MPEP 2131). Claims 6-9 inherently contain the features of claim 5. Consequently, Ajika fails to anticipate claims 6-9 for the same reason that it fails to

anticipate claim 5.

Furthermore, it is believed that claims 7 and 8 contain subject matter that is allowable over Ajika.

Claim 7 recites, *inter alia*, that the sector structure further comprises a plurality of word lines arranged in the cell array block. Contrary to this recited feature, Ajika teaches that an erase block 26 is defined to include all of a plurality of memory transistors sharing **one** word line in one erase block 26 (FIG. 2; column 7, lines 61-67; emphasis added). Consequently, Ajika fails to anticipate claim 7 for this additional reason (MPEP 2131).

Claim 8 recites, inter alia, that the write driver and the sense amplifier are configured to be placed in a state of high impedance during an erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 8 for this additional reason (MPEP 2131).

With respect to claim group C (claims 10-14), claim 10 recites, *inter alia*, a nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising a cell array block and a column decoder block. The cell array block further comprises a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate connected to a corresponding word line out of the plurality of word lines, each drain connected to a corresponding bit line out of the plurality of bit lines.

Contrary to claim 10, Ajika's erase block 26 does not comprise a plurality of bit lines, rather there is only one main bit line 24 that is connected to the select gate transistors that are located on either side of the erase block (FIGS. 2 and 3; column 7, lines 15-20). Ajika discloses that sub bit lines 19a, 19b are connected to the drains 4 of ***each*** memory transistor 11 (FIG. 2 and 3; column 6, lines 63-65; emphasis added). However, if the sub bit lines 19a, 19b are considered to be the recited plurality of bit lines then the drains of each of the memory cell transistors are not connected to a corresponding bit line out of the plurality of bit lines as recited in claim 10.

Also contrary to claim 10, Ajika's erase block 26 does not comprise a plurality of word lines (FIG. 2; column 7, lines 61-67).

Claim 10 also recites that the column decoder block further comprises a plurality of column decoder transistors, each column decoder transistor connected between a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines.

It is alleged that the select gate transistors 12 within the memory erase blocks 26 are

the recited "column decoder block." In this case, the select gate transistors are provided at both ends of the p-well region 3, on either side of the erase block 26 (FIGS. 2 and 3; column 6, lines 52-67).

Pending claims must be interpreted consistently with the specification (see, e.g., MPEP 2111). The applicants submit that the interpretation of a "column decoder block" as being the select gate transistors 12 on both sides of the erase block 26 is inconsistent with the specification, where a "column decoder block" is shown in FIG. 3 as a singular, contiguous area 103, and not as plural areas separated by the erase block 26 as shown in Ajika FIG. 2 and 3. In other words, the applicants have claimed a single "column decoder block" having a plurality of column decoder transistors, and not multiple "column decoder blocks" that each have a single select gate transistor.

Furthermore, even if the two select gate transistors 12 shown at either side of the erase block in Ajika FIG. 2 and 3 could be considered a "column decoder block," each of Ajika's select gate transistors 12 is not connected to a corresponding bit line out of the plurality of bit lines as required by claim 10. Rather, both of Ajika's sub bit lines 19a, 19b are connected to one n-type impurity region 15b of the select gate transistor via a contact hole 17 (column 6, lines 65-67), while the other n-type impurity region 15a of the select gate transistor is connected to the main bit line 24 through a contact hole 16 (column 7, lines 17-20). In other words, only one main bit line 24 is connected to the select gate transistors 12 in Ajika's "column decoder block", not a plurality of bit lines. It was explained above why Ajika's sub bit lines 19a, 19b cannot be considered the recited plurality of bit lines.

Because Ajika fails to teach the elements of claim 10 discussed above, Ajika does not anticipate claim 10 (MPEP 2131). Claims 11-14 inherently contain the features of claim 10, consequently, claims 11-14 are also not anticipated by Ajika (MPEP 2131).

Furthermore, it is believed that claim 14 contains subject matter that is allowable over Ajika.

Claim 14 recites that the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation. Ajika does not teach this feature, consequently Ajika does not anticipate claim 14 for this additional reason (MPEP 2131).

With respect to claim group D (claims 15-17 and 27), independent claim 15 has been alleged to be anticipated by Ajika FIG. 8. While the comments previously presented for claim 15 with respect to Ajika FIG. 8 still apply, the same comments can not be made with

respect to Ajika FIG. 1.

However, claim 17 recites that the transistors of the column decoder (claim 15) comprise a column decoder block. As was explained above, Ajika's select gate transistors 12 are found on opposite sides of the erase block 26, thus they cannot be considered the recited column decoder block. Consequently, Ajika fails to anticipate claim 17 (MPEP 2131). Assuming that this argument proves persuasive to the Board, the applicants propose amending claim 15 to incorporate this subject matter.

Furthermore, claim 27 recites that the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one. Ajika does not teach these features. For example, Ajika does not show a column decoder block arranged in at least a (1 x 2) array, neither does it show a cell array block arranged in at least a (2 x 2) array. Consequently, Ajika fails to anticipate claim 27 (MPEP 2131).

With respect to claim group E, claim 18 recites, similar to claim 27, a cell array block arranged in a (M x N) array, where M and N are at least equal to 2, and a column decoder block arranged in a (P x N) array, where P is at least equal to 1. Ajika does not teach this feature, consequently, Ajika fails to anticipate claim 18 (MPEP 2131).

Claims 19 and 20 inherently contain the features recited in claim 18. Consequently, Ajika fails to anticipate claims 19 and 20 for the same reason as claim 18.

IX. APPENDIX
37 CFR §1.192(c) (9)

1. (Previously presented) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sectors on the substrate;

each sector comprising memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block;

wherein the transistors in the cell array block and column decoder block in each sector share a common bulk region, wherein the common bulk region is formed on the substrate and is connected to a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of the sector; and

wherein said semiconductor memory device is configured to electrically erase all the

memory cell transistors in a sector together.

2. (Original) A nonvolatile semiconductor memory device according to claim 1, wherein the semiconductor memory device is a NOR-type memory device.

3. (Original) A nonvolatile semiconductor memory device according to claim 1, further comprising a write driver and a sense amplifier.

4. (Original) A nonvolatile semiconductor memory device according to claim 3, wherein the write driver and sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation.

5. (Original) A sector structure of a nonvolatile semiconductor memory, said sector structure comprising:

a plurality of memory cell transistors arranged in a cell array block; and

a plurality of decoder transistors arranged in a column decoder block, wherein said memory cell transistors and decoder transistors are arranged on a common bulk region.

6. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein an erase operation is configured to erase all of the transistors in the sector simultaneously.

7. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, said sector structure further comprising:

a plurality of word lines arranged in the cell array block, each word line being connected to a plurality of cell gates;

a plurality of bit lines arranged in the cell array block, each bit line being connected to a plurality of memory cell drains;

a plurality of common data lines connected to the bit lines;

a plurality of write drivers, each connected to a respective one of the common data lines; and

a plurality of sense amplifiers, each connected to a respective one of the common data

lines.

8. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 7, wherein each write driver and sense amplifier is configured to be placed in a state of high impedance during an erase operation.

9. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein said sector structure is configured to provide 64 Kbytes of memory.

10. (Previously Presented) A nonvolatile semiconductor memory device with a plurality of sectors, each sector comprising:

a cell array block comprising a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of the plurality of word lines, each drain being connected to a corresponding bit line out of the plurality of bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors and configured to apply a source voltage;

a column decoder block comprising a plurality of column decoder transistors, each column decoder transistor connected a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines; and

a common bulk region arranged in each sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors in each sector share the common bulk region; and

a bulk driver provided in each of the sectors, each said bulk driver configured to commonly apply a bulk voltage to the common bulk region of that sector.

11. (Original) A nonvolatile semiconductor memory device according to claim 10, wherein the memory device is a NOR-type flash EEPROM.

12. (Original) A nonvolatile semiconductor memory device according to claim 10, wherein the bulk region is a pocket P-well.

13. (Original) A nonvolatile semiconductor memory device according to claim 10, further comprising a plurality of write drivers and sense amplifiers, wherein each data line is connected to a corresponding one of the write drivers and a corresponding one of the sense amplifiers.

14. (Original) A nonvolatile semiconductor memory device according to claim 13, wherein the write drivers and sense amplifiers are each configured to be placed in a state of high impedance during an erase operation.

15. (Previously presented) A nonvolatile semiconductor memory device comprising:

a substrate;

a plurality of sector units, each sector unit comprising a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, and wherein each sector unit is configured to be electrically erasable in response to an erase signal; and a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage.

16. (Original) A nonvolatile semiconductor memory device according to claim 15, wherein each sector unit further comprises a bulk driver configured to supply a bulk voltage to the common bulk region.

17. (Original) A nonvolatile semiconductor memory device according to claim 15, wherein said plurality of memory cell transistors are arranged in a cell array block, wherein said plurality of column decoder transistors are arranged in a column decoder block, and wherein said cell array block and said column decoder block are both arranged on the common bulk region.

18. (Previously presented) A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:

forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the cell array block is arranged in an (M x N) array with M and N both at least equal to two; and

forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder is arranged in a (P x N) array with P at least equal to one.

19. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, further comprising configuring the bulk regions for the memory cell transistors and decoder transistors to receive a common bulk signal during an erase operation.

20. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, wherein said memory cell transistors and said decoder transistors are configured to be simultaneously erased with each other during an erase operation.

21-25. (Not entered)

26. (Previously presented) The device of claim 1, wherein the cell array block and the column decoder block of each sector share a plurality of word lines and a plurality of bit lines.

27. (Previously presented) The device of claim 17, wherein the cell array block is arranged in a (M x N) array and the column decoder block is arranged in a (P x N) array, where M and N are at least equal to two and P is at least equal to one.

CONCLUSION

The Appellant requests favorable consideration by the Board. If any questions remain, please call the undersigned.

Respectfully submitted,

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Adrienne Chocholak

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PATENT APPLICATION
Docket No. 5484-093
Client No. PX1392-US/SSD

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Byeong-Hoon Lee and Seung-Keun Lee		
Serial No.	09/997,080	Examiner:	Phan, Trong Q
Filed:	November 28, 2001	Art Unit:	2818
For:	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE		
Confirmation No.:	6095		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Enclosed for filing in the above-referenced application are the following:

☒ Appellant's Brief under 35 CFR § 1.192 (in triplicate).
☒ PTO Form 2038 authorizing credit card payment of $330.00 filing fee for brief in support of appeal is enclosed.
☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Customer No. 20575

Respectfully submitted,

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